Nano-crystalline Oxide Semiconductor Materials for Semiconductor and Display Technology

Sanghun Jeon Ph.D. Associate Professor

Department of Applied Physics
Korea University

Personnel Profile (Affiliation and Employment)

Affiliation

Associate Professor in the Department of Applied Physics at Korea University

Education

03 Ph.D. Electronic Materials (Semiconductor Device, MOS dev. & Tr. Tech
(w/ Best Paper Award & Young Researcher Award)
Young Researcher Award at Int. Conf. on SSDM Nagoya Japan 2002)

Employment

~ 10 Yr experience at Samsung Adv. Inst. Tech., and Samsung Electronics in Semiconductor Area for Last a Decade with 6 research awards.

12~ **Samsung Adv. Inst. Tech., SEC. Principal Research Staff Member**

Project leader of Haptic materials and devices (Tactile sensor)

09~11 **Samsung Adv. Inst. Tech., SEC. Principal Research Staff Member**

Ox-based Device, Lead Device Physicist and Process Integrator

Photo/Image Sensor, Interactive Display, Integrated Circuits, High Power Device Transparent device, 3D device, Electrical/Reliability/Modeling works.

05~09 **Memory Business Division of SEC, Senior Research Staff Member**

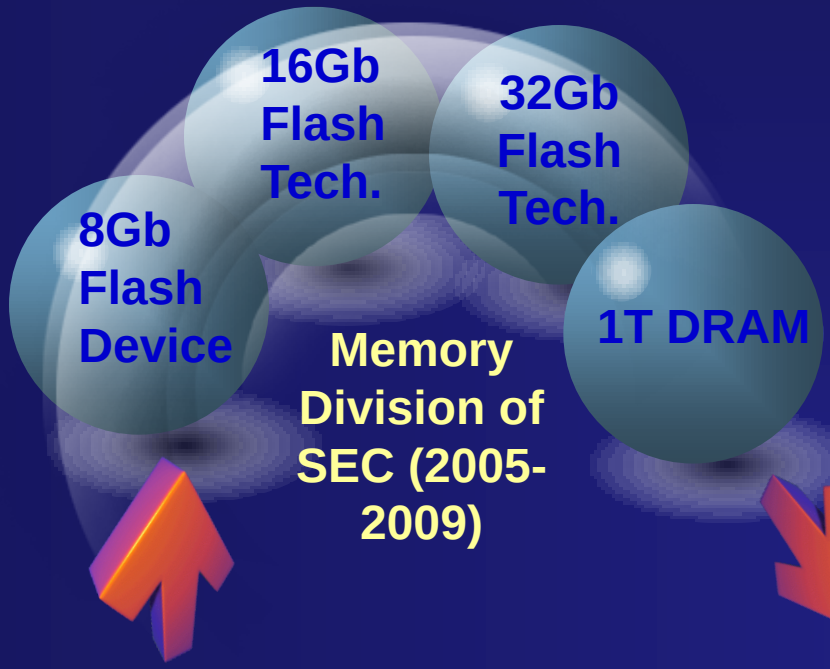
Charge Trap Flash (8, 16, 32Gb). Process Integrator and Device Engineer.

03~05 **Samsung Adv. Inst. Tech., [SAIT] Senior Research Staff Member**

Initiative Study on Charge Trap Flash Memory Device.

Technology Transfer @ Samsung

Two-time tech. transfer from SAIT to business divisions of SEC, memory division (2005-2009) and display division (2011)



Display Division of SEC (2011)

SAIT (2003-2005) Tech. Transfer

Basic Research on CTF → Meeting Specification of NAND for 40nm gen.

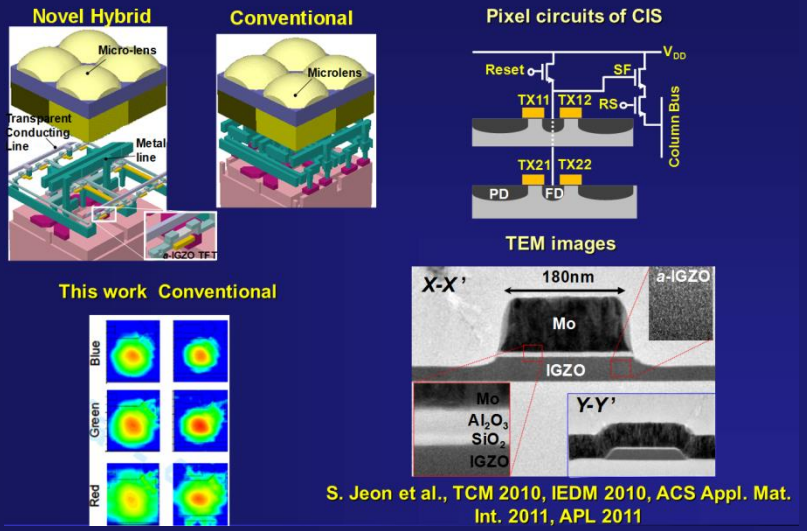
SAIT (2009-2012)

Understanding on science of oxide → Demonstration of Ox. Sensor Array → Various Sensors for E-Body

Contents

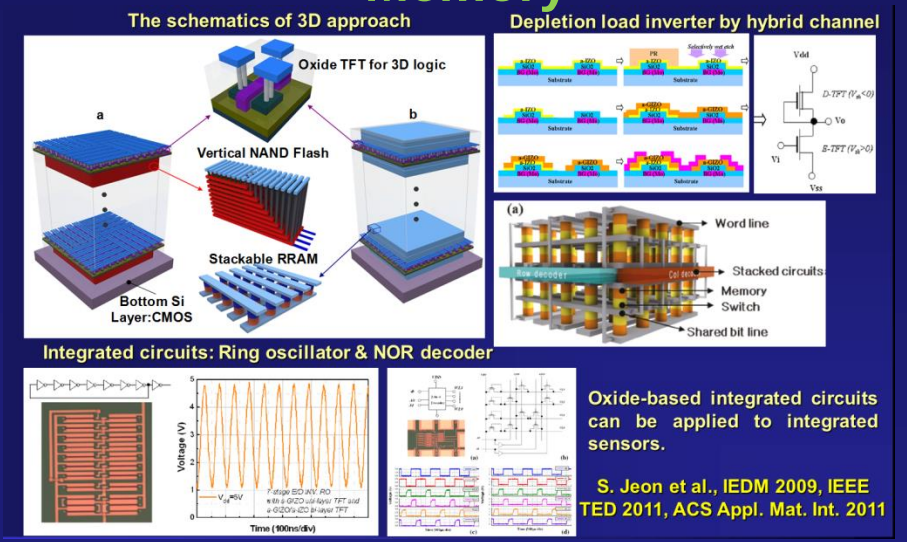
For nc-ox. device, I present various applications.

Image Sensor



S. Jeon et al., TCM 2010, IEDM 2010, ACS Appl. Mat. Int. 2011, APL 2011

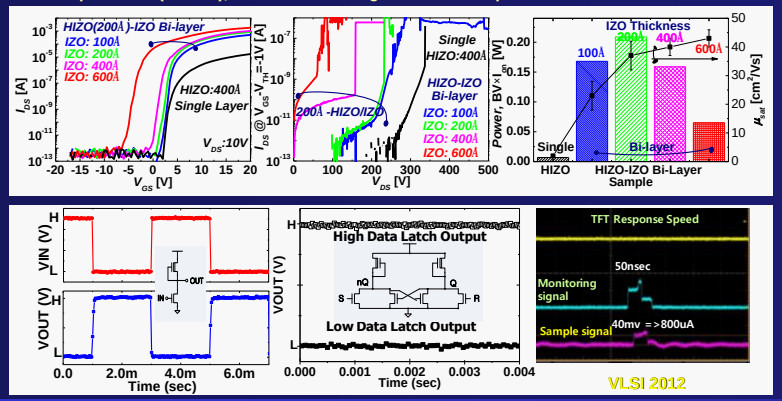
Memory



S. Jeon et al., IEDM 2009, IEEE TED 2011, ACS Appl. Mat. Int. 2011

Power

Bilayer oxide transistor exhibits remarkable performance such as, high mobility (23~47cm²/Vs) and high breakdown voltage (BV) of 60~340V despite low process temperatures (<300°C), which can be integrated on metal pad.



VLSI 2012

Display

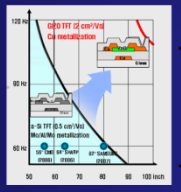
Motivation of oxide photo-sensor

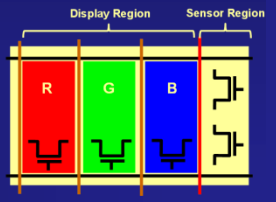
⇒ Large Area Interactive Display

- Display size is limited by driving speed. μ > 5 cm²/eV/s for UD-level

∴ High μ oxide TFT for display

- Process compatibility: oxide sensor

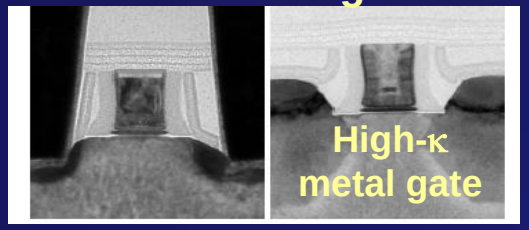




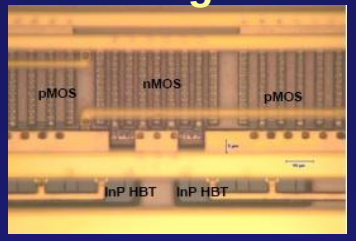
The Evolution of Devices

- CMOS Logic Device (Si → III-V/ Graphene on Si)

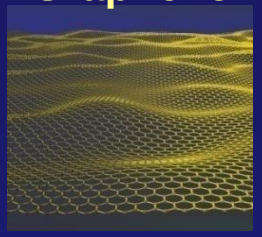
Si based Integration



III-V Integration

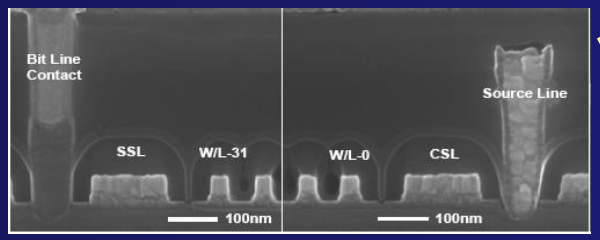


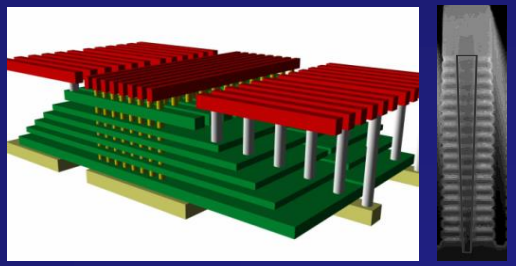
Graphene



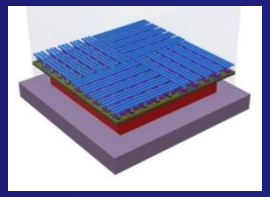
- Memory (Planar →Vertical/Hybrid Integration)

Planar Structure, IEDM 2006

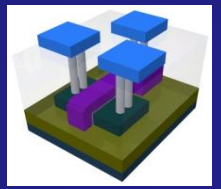


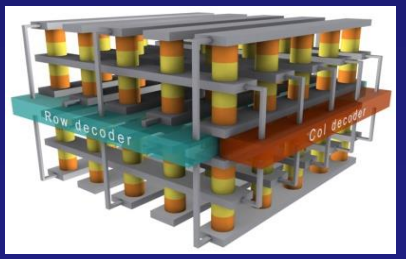


VNAND, VLSI 2009



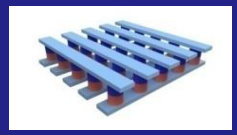
AOS TFT





RRAM, Adv. Fuct. Mat. 2008

Transition Ox. Based RRAM

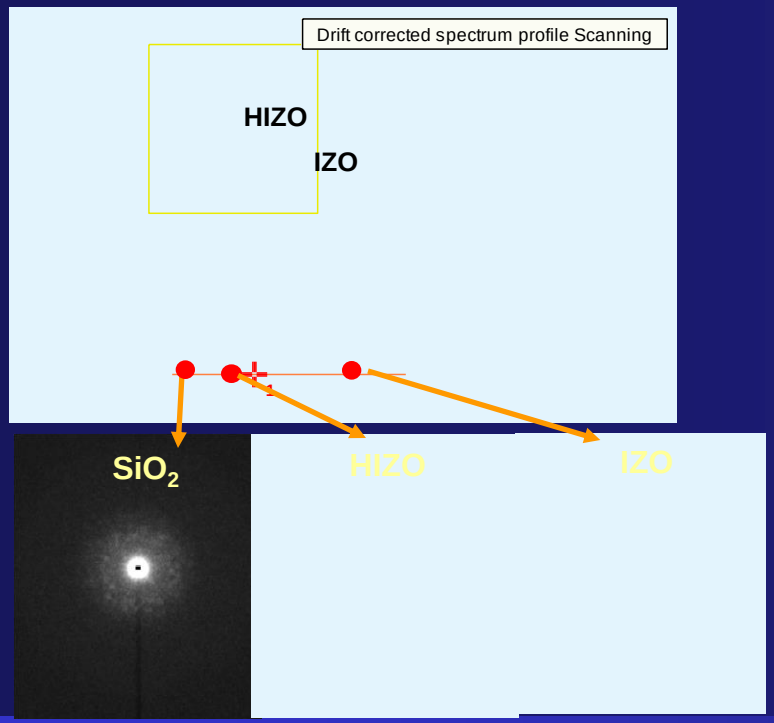


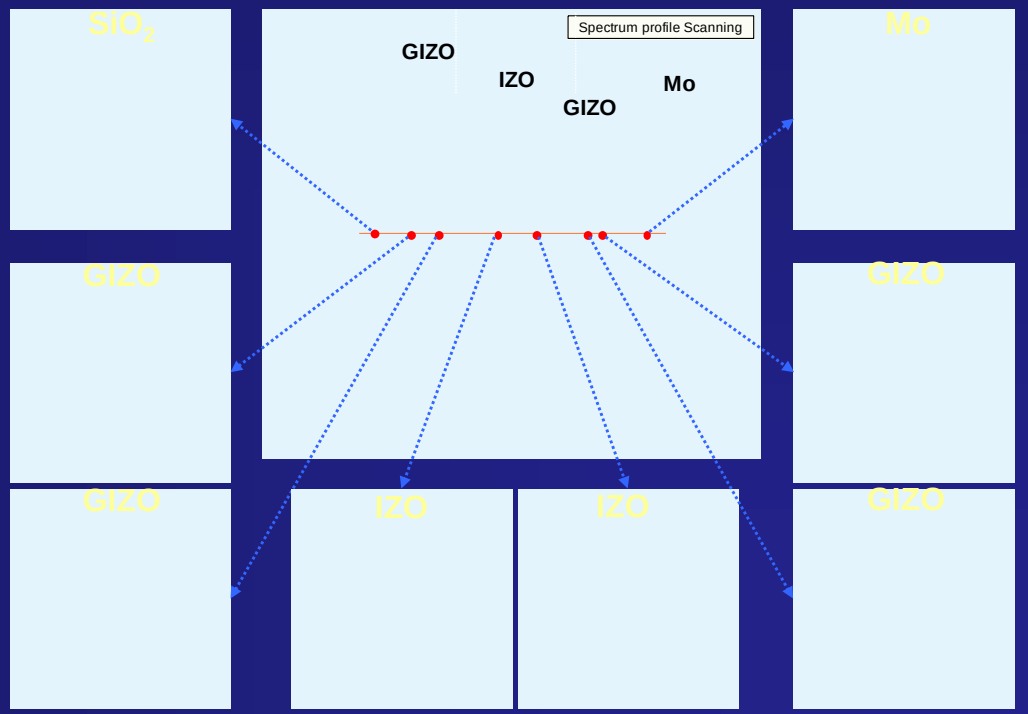
Key Trend: Alternative Materials and 3D Stack

Benefit of nc-InGaZnO, nc-HfInZnO, and nc-InZnO

- Optical transparency due to large band-gap of ~3.4eV
- Stackable process nature due to low temp. process capability
- Nano-crystalline structure in amorphous matrix (negligible ΔV_{th}) but High μ (>10)

→ The integration of *nc*-oxide semiconductor onto Si circuits is possible.

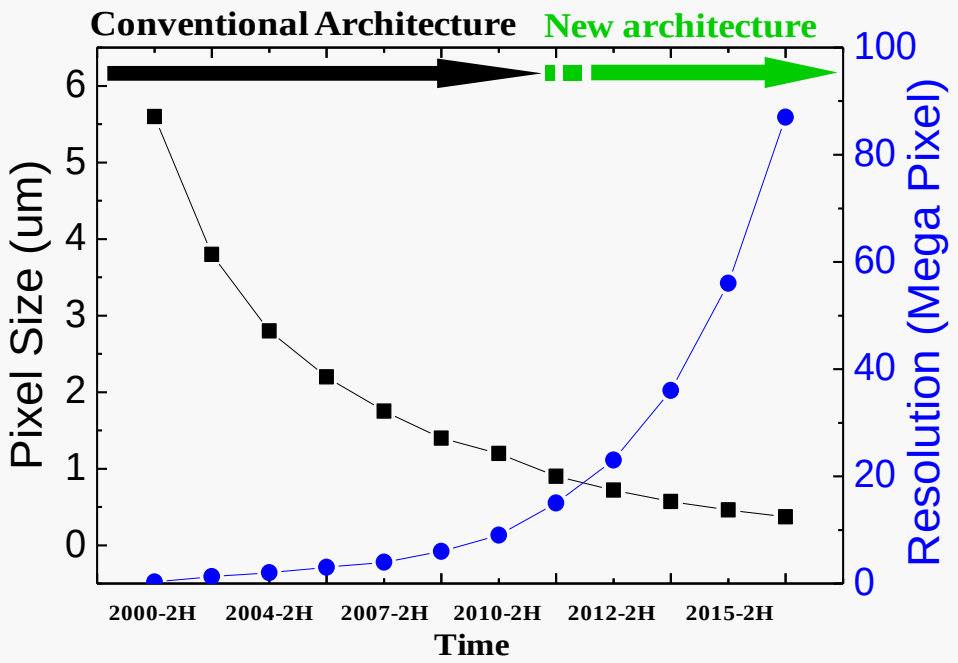




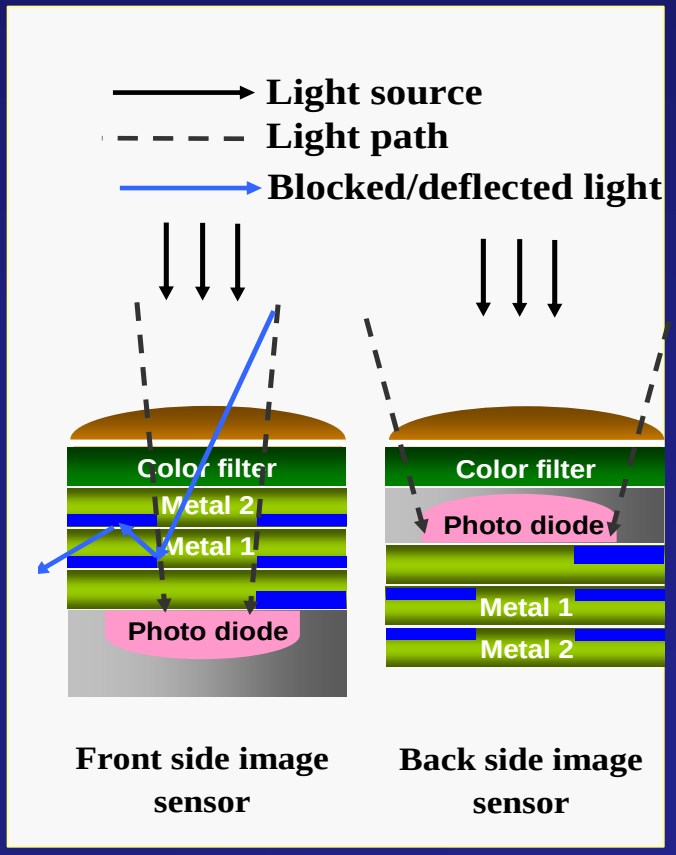
CMOS Image Sensor Applications

Current Status of CIS Devices

- Like others, CIS devices are facing physical limitation
- Shrinking the pixel size is a major driver for imaging business
- Pixel performance is inversely proportional to the size of CIS
- At a pace which counteract both, new technique is needed



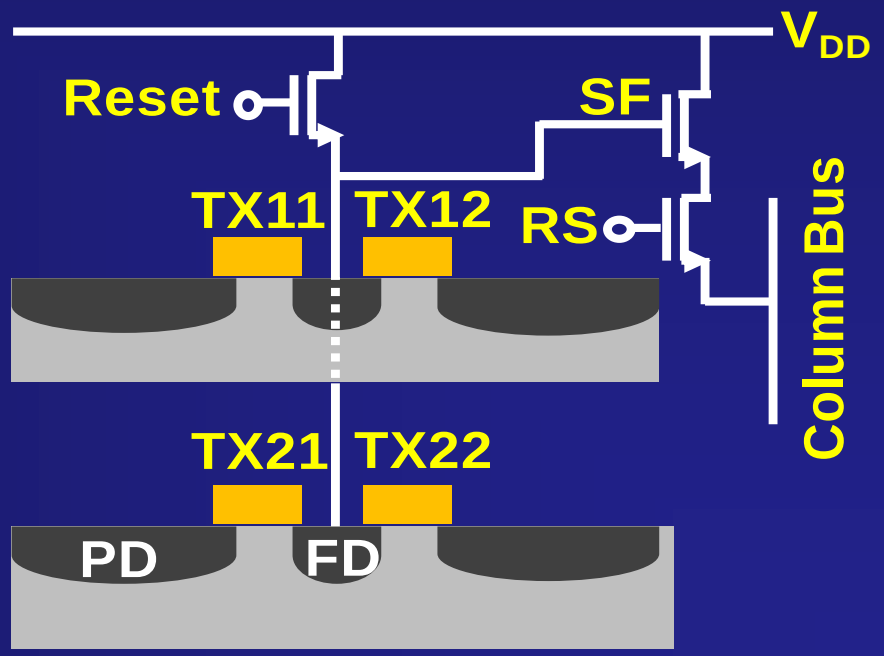
FSIS: Front side image sensor BSIS: Back side image sensor



Pixel Circuit of CMOS Image Sensor

- A pixel consists of 1 Photodiode (PD) and 4 Transistors.
- Pixel Tr.s (Reset, SF, RS) are shared with neighboring pixels
- Interestingly, all pixel transistors are NMOSFET
- Pixel Tr.s (Reset, SF, RS) with less stringent requirement can be replaced with oxide TFT

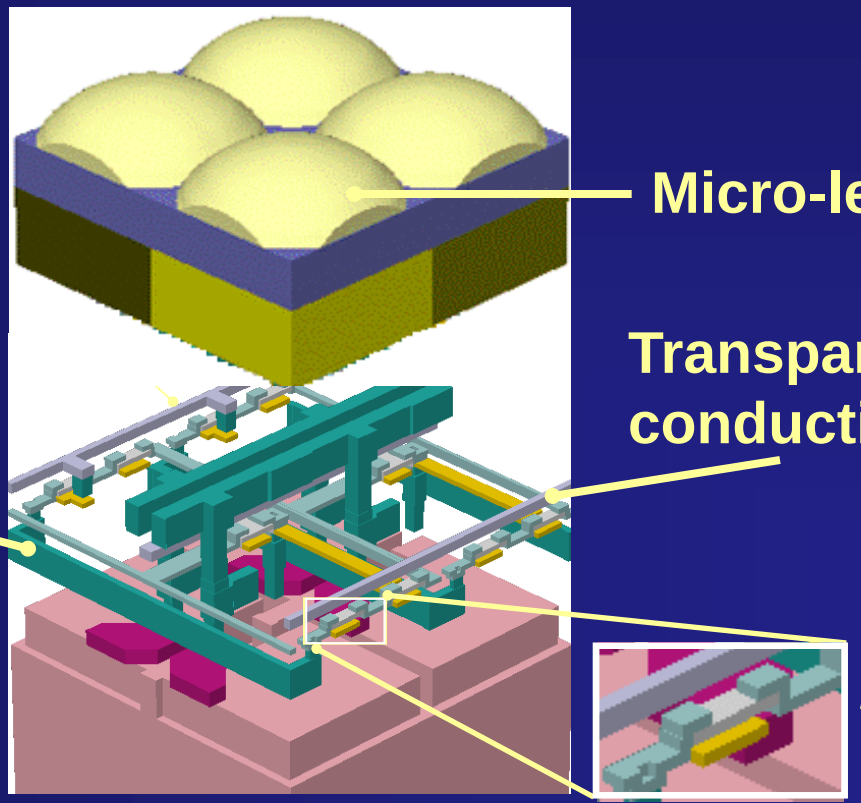
TX: Transfer Gate Transistor
Reset: Reset Transistor
SF: Source Follower Transistor
RS: Row Select Transistor
PD: Photodiode
FD: Floating Diode



Our Approach

- The integration of electronically active oxide device onto silicon circuit.
- Here we propose a novel hybrid CIS architecture utilizing nanometer scale nano-crystalline oxide TFT with a photodiode.

S. Jeon et al., ACS Applied Mat. Int. 2011
S. Jeon et al., IEEE IEDM 2010

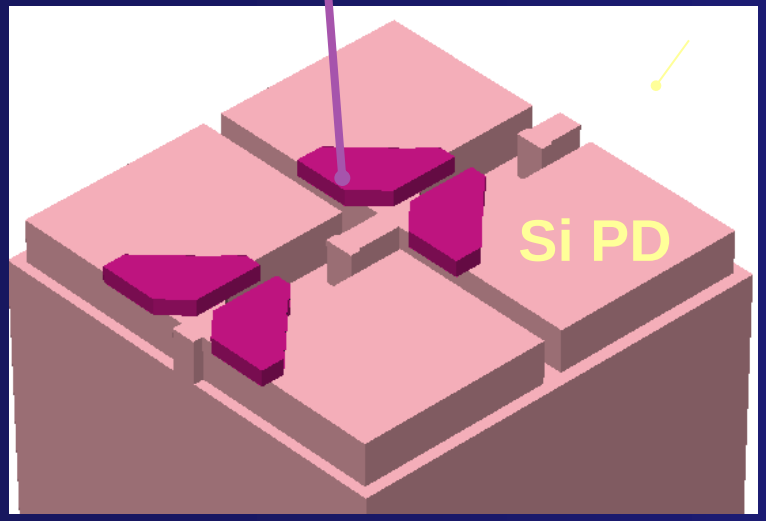


Structural Comparison (1st layer)

- This demonstrates how Si PD in active can be enlarged.

Novel Hybrid

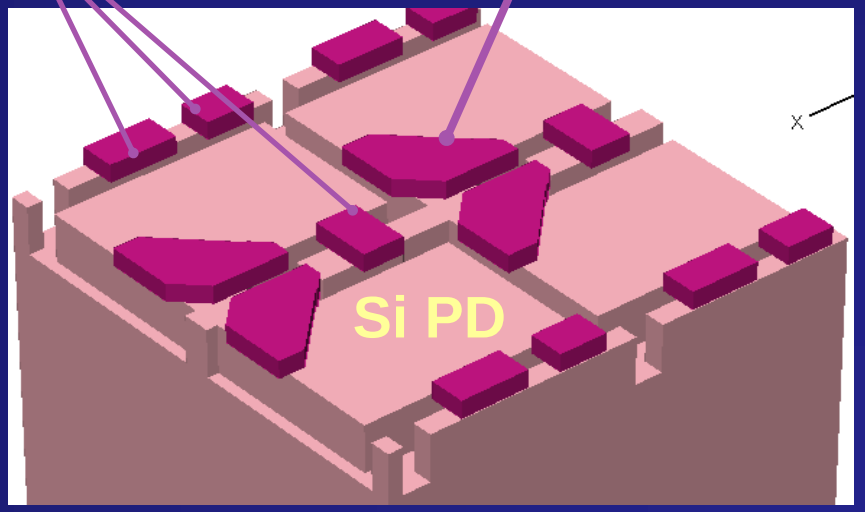
Transfer Gate Si Transistor



Conventional

Other Pixel Transistors

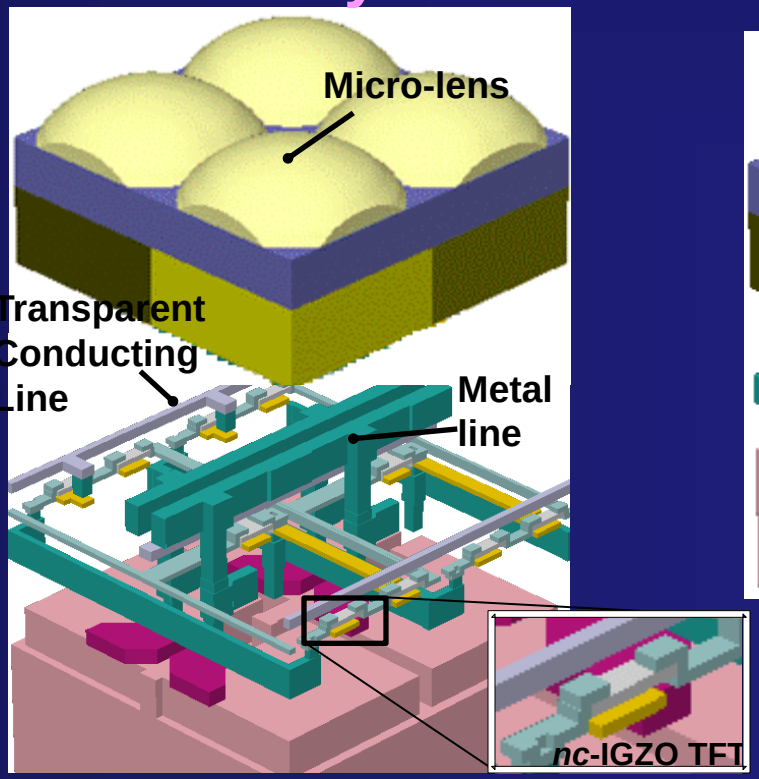
Transfer Gate Transistor



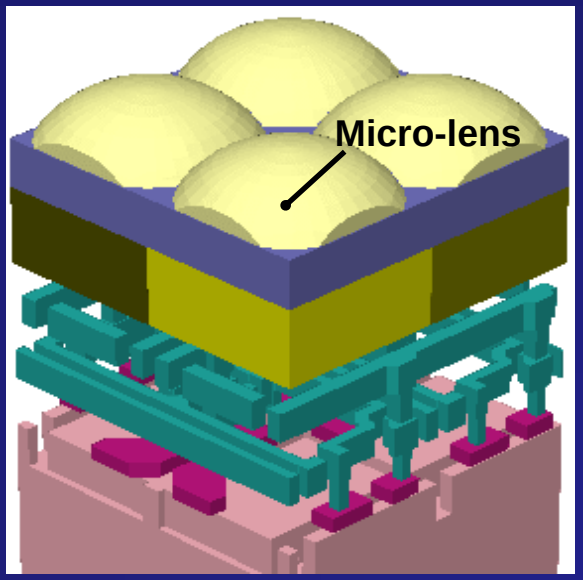
Structural Comparison (2nd layer)

- The 2nd layer of a novel hybrid four-pixel CIS structure consists of inter-connect metal lines and other pixel transistors.
- Some interconnect metal lines for delivering constant voltage, V_{DD}, are replaced by a TCO

Novel Hybrid

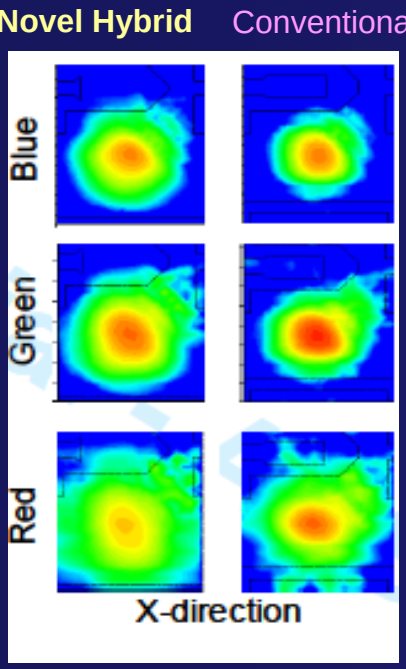


Conventional



Simulation Results

- Electromagnetic power density contour plots were calculated by Sentaurus electromagnetic solver.
- The simulation results reveals a quantum efficiency increase of 143% 116%, and 120% at blue, green, and red wavelengths, respectively.

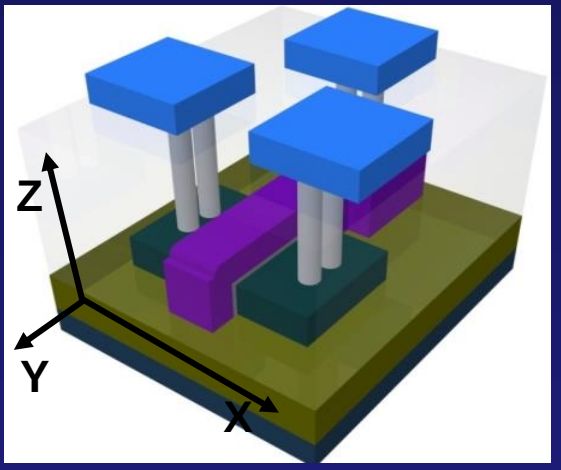


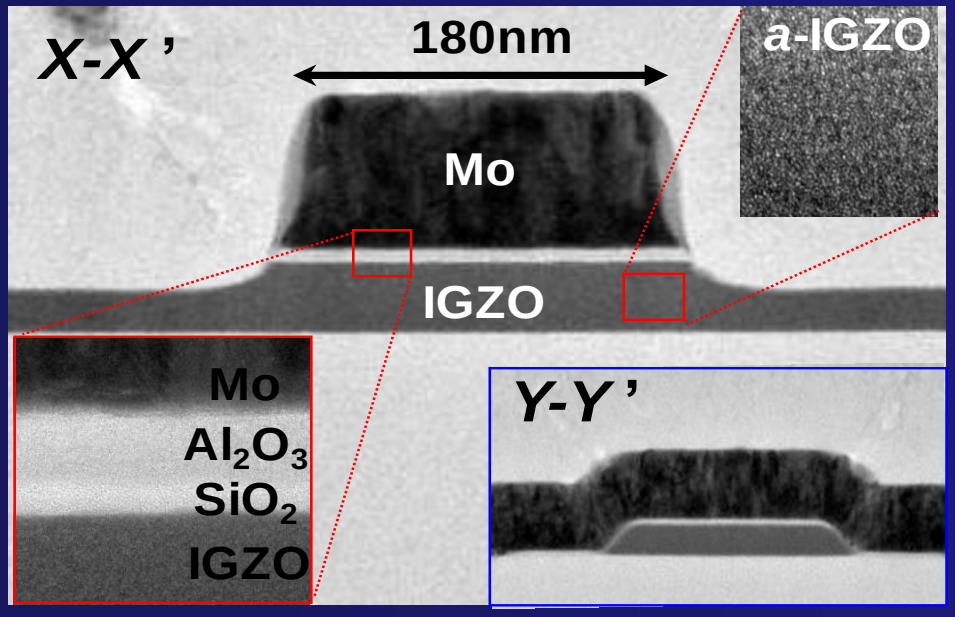
Pixel	Wavelength (nm)	Quantum Efficiency (%)	Ratio (%)
Conventional	450	34.3	-
Hybrid + TCO Interconnect Line		49.2	143
Conventional	540	61.9	-
Hybrid + TCO Interconnect Line		71.5	116
Conventional	650	41.3	-
Hybrid + TCO Interconnect Line		49.4	120

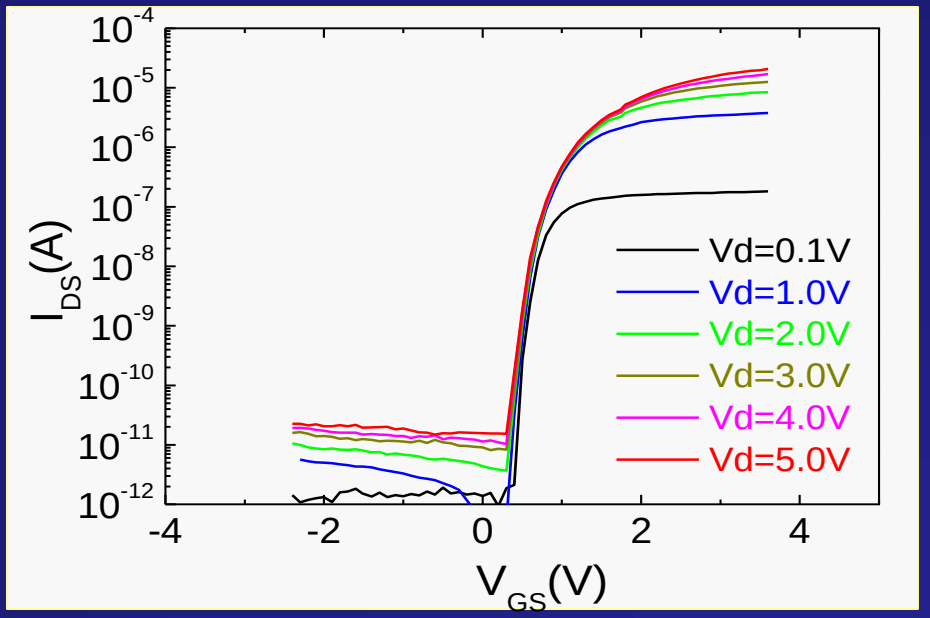
Structural Analysis & Electrical Analysis

- Self aligned top gate structure
- Dual gate stack (SiO_2/Al_2O_3)
- Trapezoidal active channel
- nc-oxide semiconductor

S. Jeon et al., Applied Physics Letters 2011







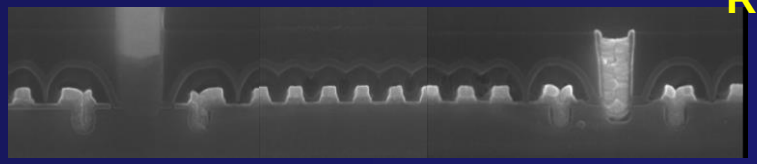
Memory Applications

Essential Device Architecture for V-NAND

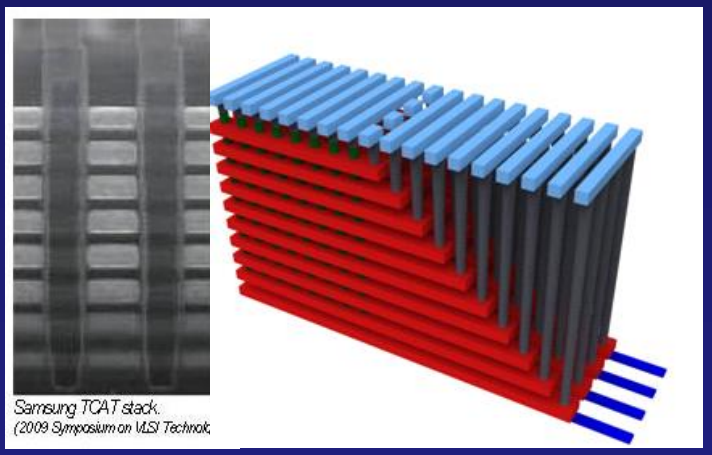
Even with revolutionary transition, the core stack remains the same.

Vertical NAND for 1 terabit and beyond

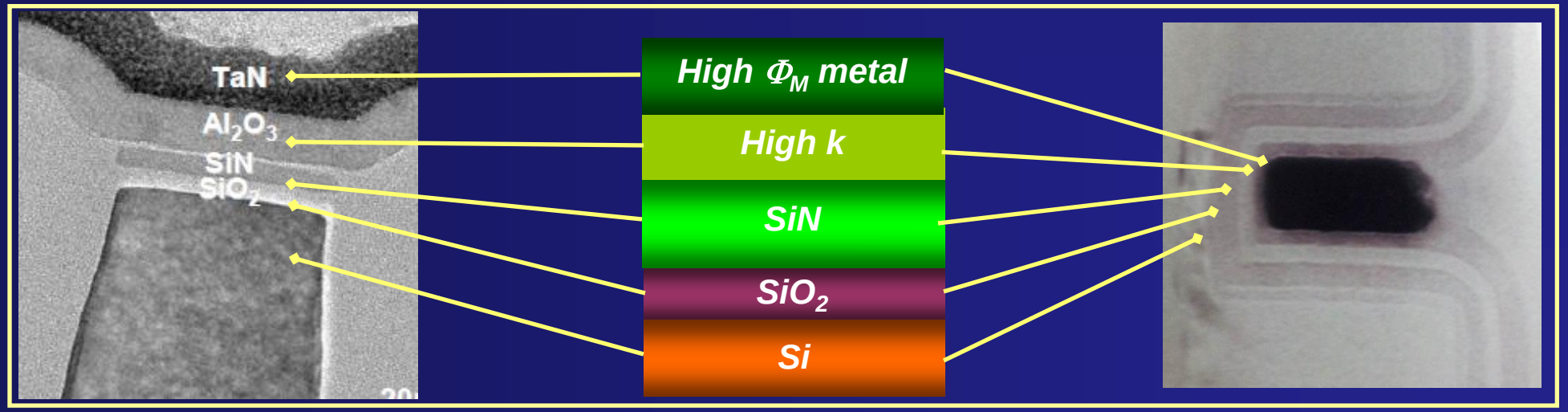
Planar NAND



Revolutionary Transition

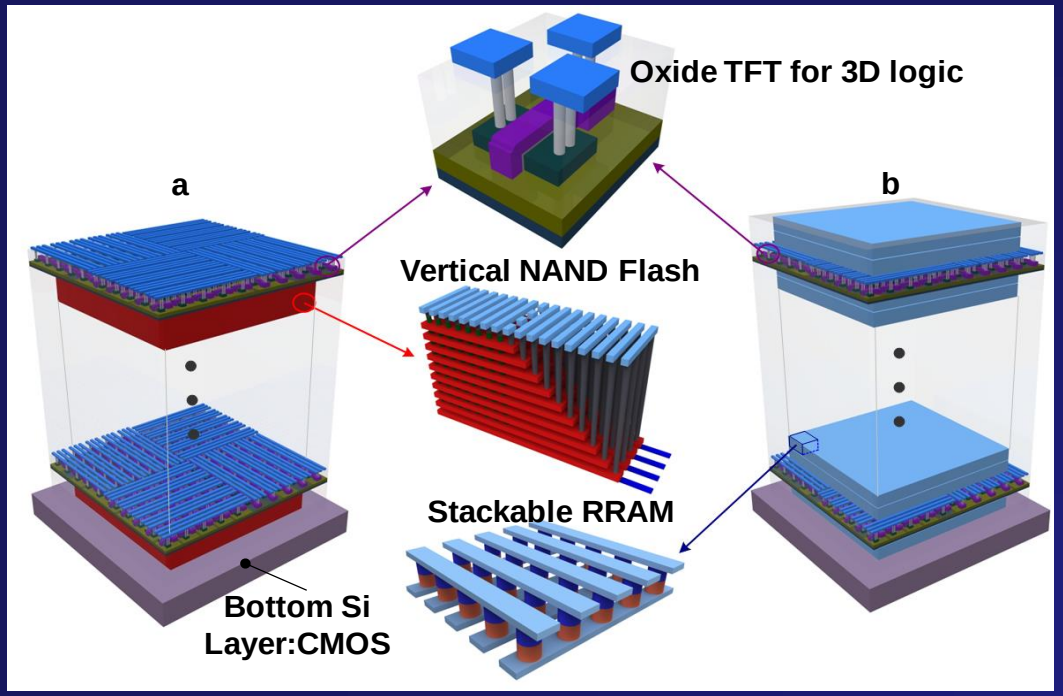


Core CTF Stack for Vertical NAND
S. Jeon et al., US 7,391,075

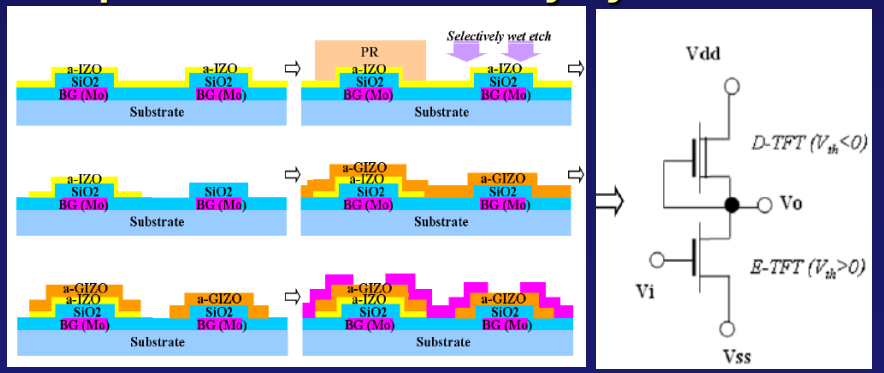


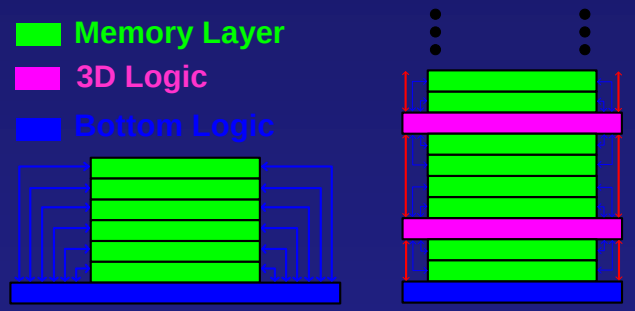
Three dimensional approach to high density memory

The schematics of 3D approach



Depletion load inverter by hybrid channel

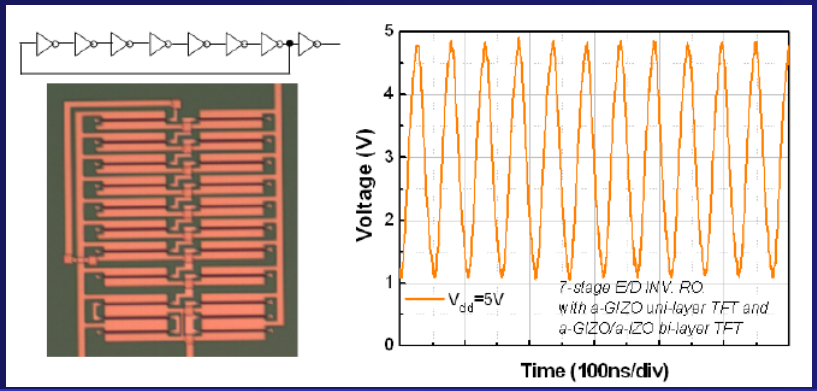


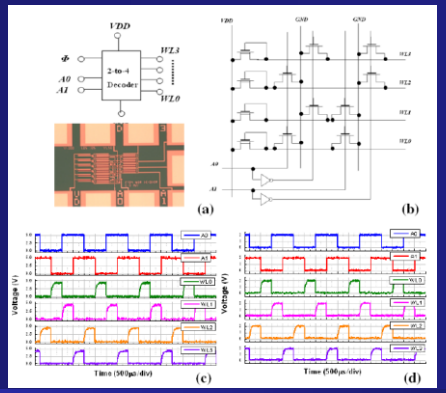


Conventional Architecture

3D Logic Architecture

Integrated circuits: Ring oscillator & NOR decoder





Oxide-based integrated circuits can be applied to integrated sensors.

IEDM 2009, IEEE TED 2011, ACS Appl. Mat. Int. 2011

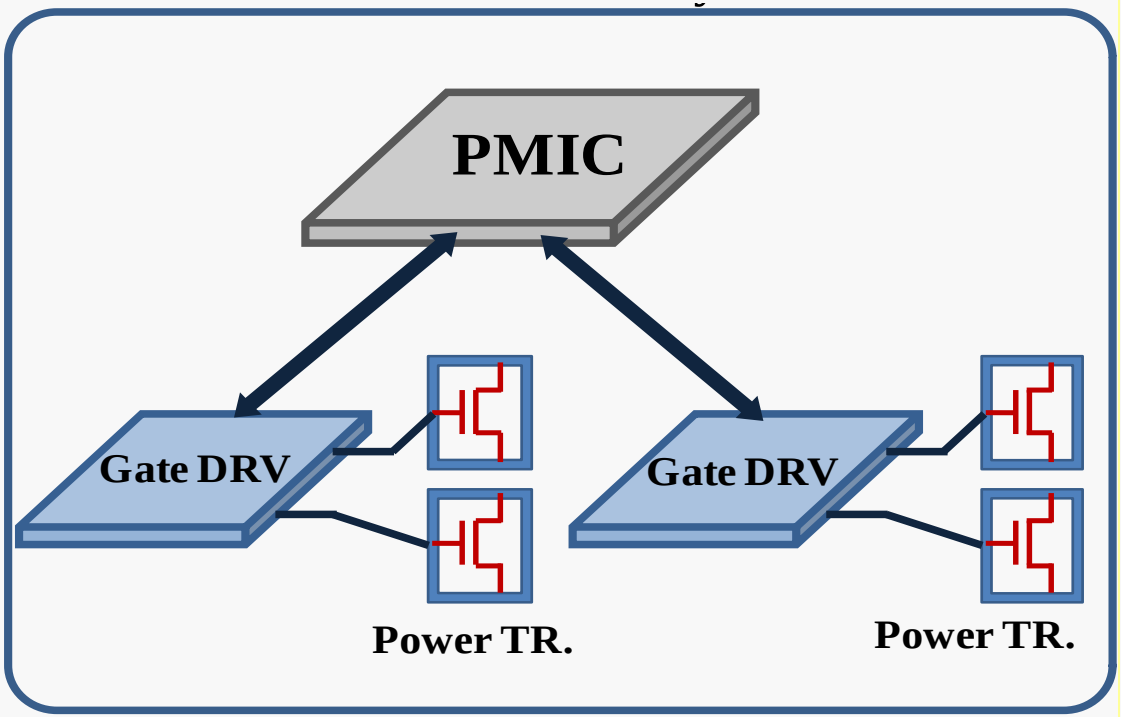
Power Applications

Conventional Power and This System

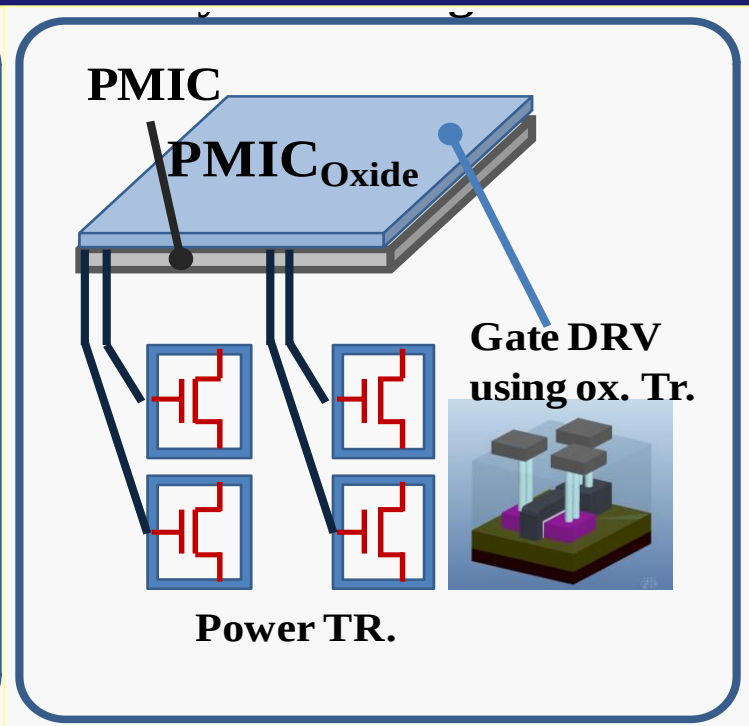
Different device specifications of PMIC & gate driver hinders on-chip integration even with the merits, such as low cost, reduced form factor, and low noise.

S. Jeon et al., VLSI 2012

Conventional Power System

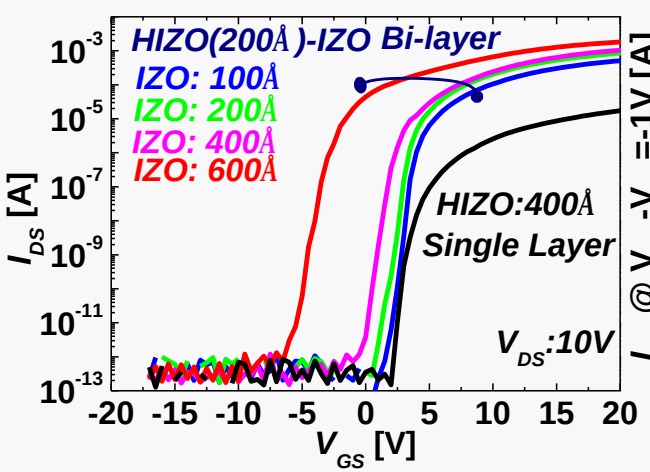


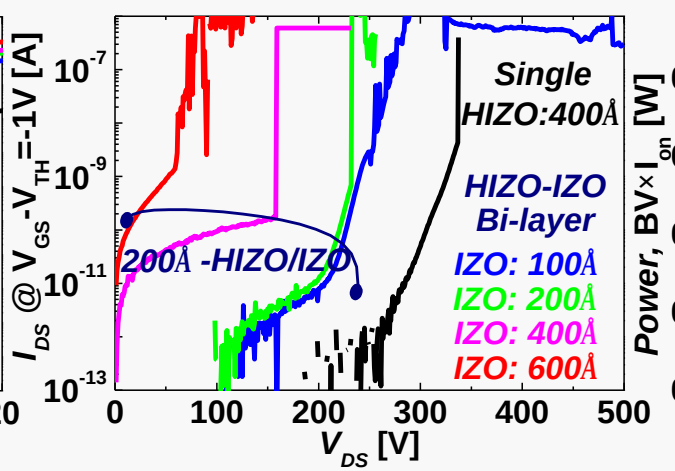
Currently Proposed System

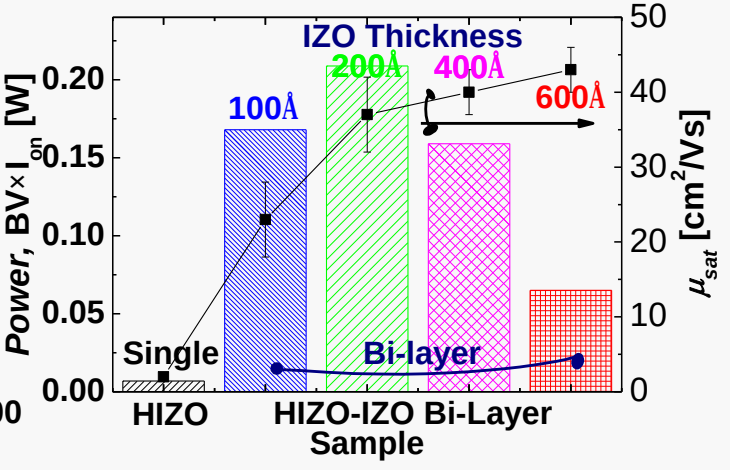


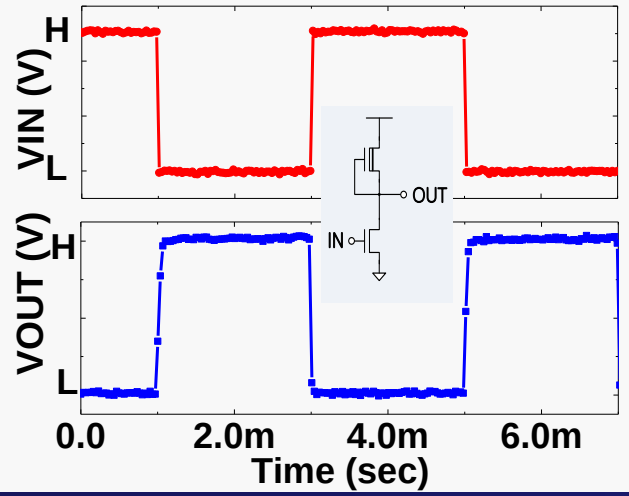
High Power Oxide Transistor Technology

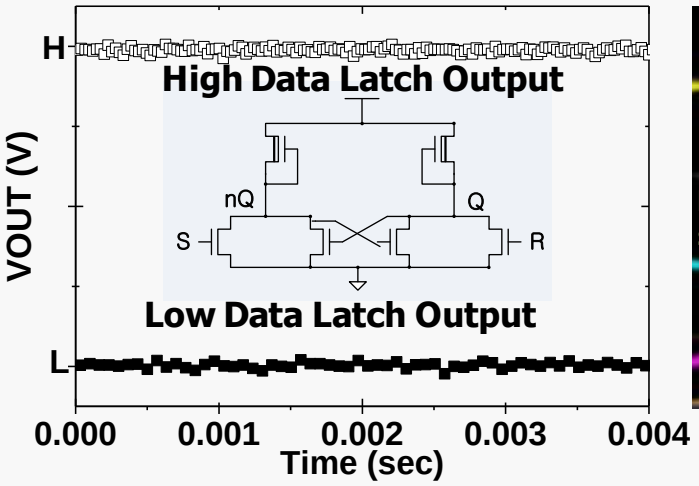
Bilayer oxide transistor exhibits remarkable performance such as, high mobility (23~47cm²/Vs) and high breakdown voltage (BV) of 60~340V despite low process temperatures (<300˚C), which can be integrated on metal pad.

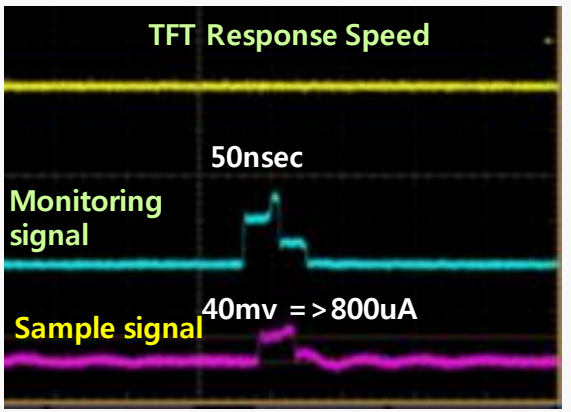












VLSI 2012

Display Applications

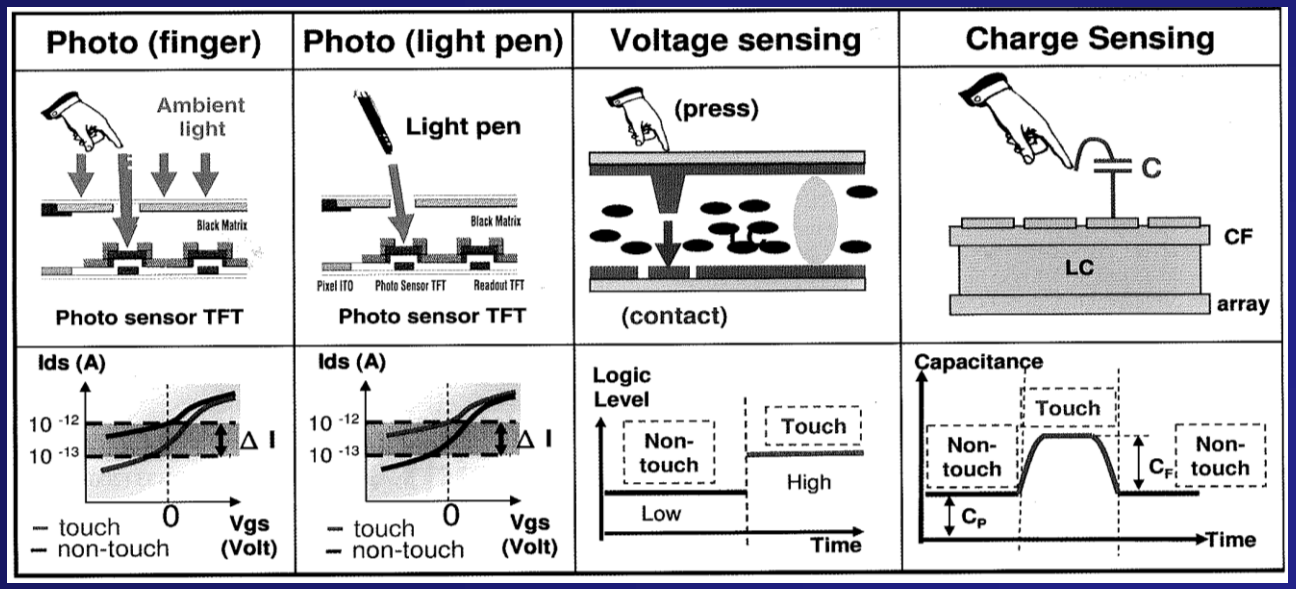
In-cell touch technologies

- Displays with touch functionality are in great demand.

" In-cell touch display" is an industrial goal (integration of sensor into LCD cell)

- Even with various approaches, there is no clear solution to realize large area interactive display.
- Previous photo-sensor technologies based on α-Si are not applicable for large area touch screen due to low speed.

Information Display 2010

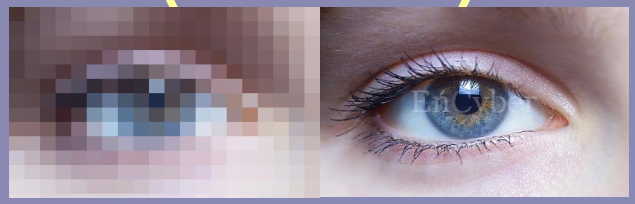


Motivation of oxide photo-sensor

⇒ Large Area Interactive Display

Large size

High resolution (FHD→UD)

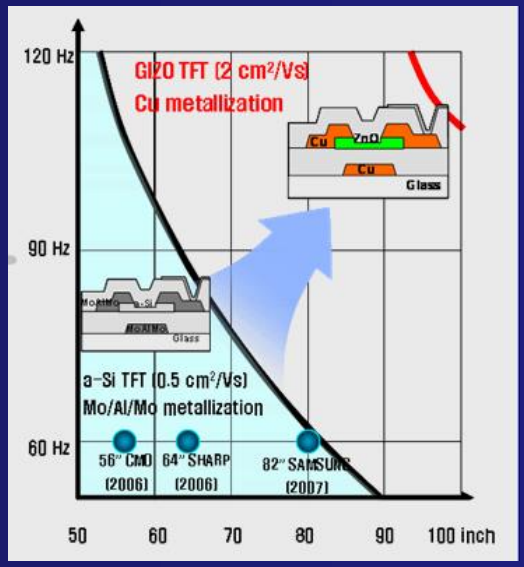


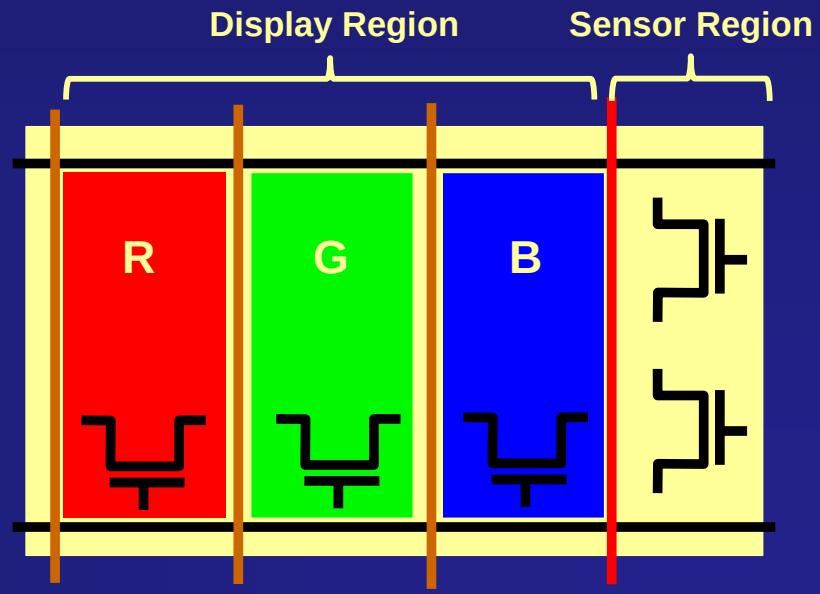
Motion picture (>120Hz)

- Display size is limited by driving speed. $\mu > 5$ $cm^2/eV/s$ for UD-level

∴ High μ oxide TFT for display

- Process compatibility: oxide sensor



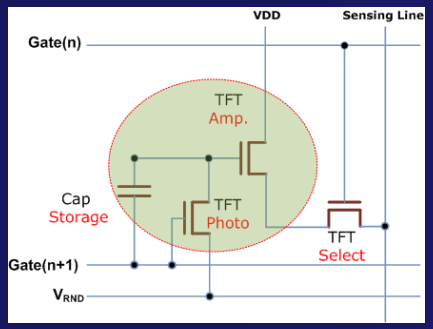


Gated Three Terminal Sensor Architecture

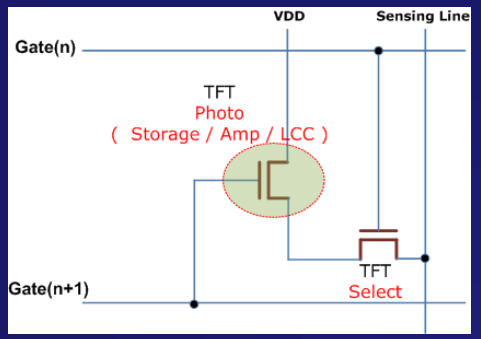
- High photo-current for oxide sensor leads to simple pixel structure
- 2 TFT architecture: One sensor TFT & one switch TFT (Shield Metal)
- Transparent photo-sensor array due to simple structure

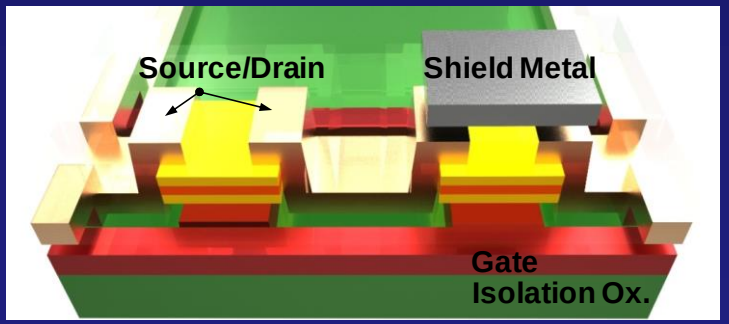
S. Jeon et al., Nature Materials 2012
S. Jeon et al., Adv. Mat. 2012
S. Jeon et al., IEEE IEDM 2010
S. Jeon et al., IEEE IEDM 2011

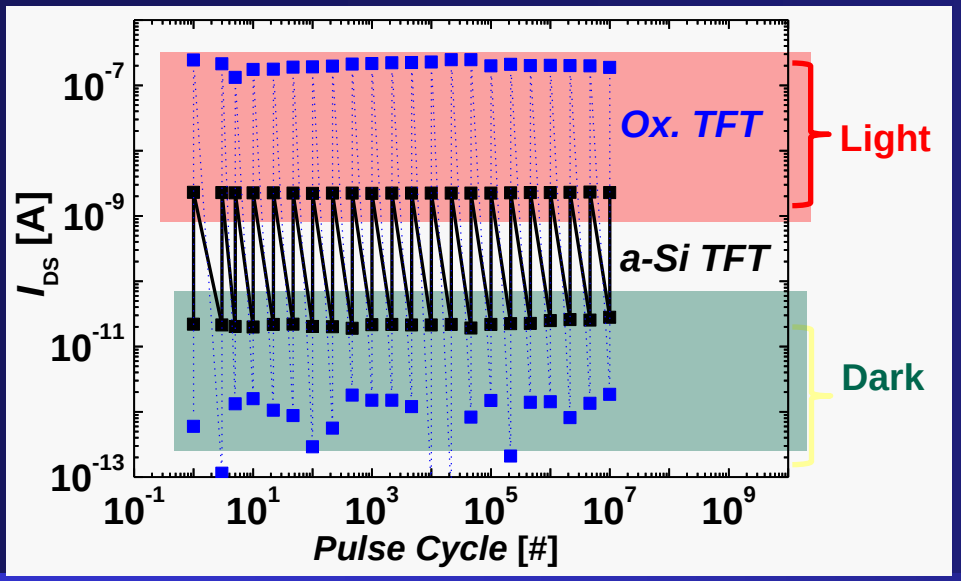
a-Si Photo TFT array



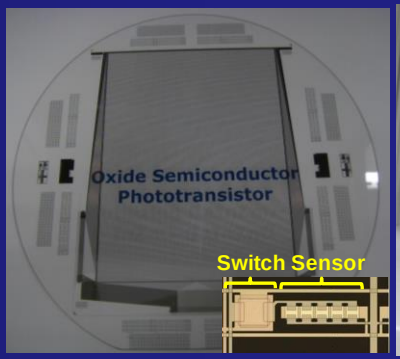
Oxide Photo TFT array

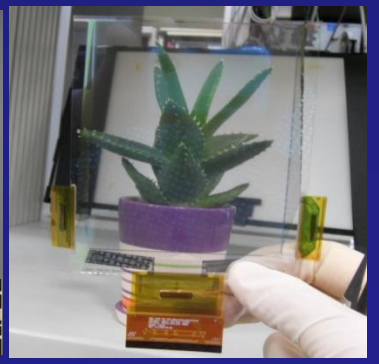






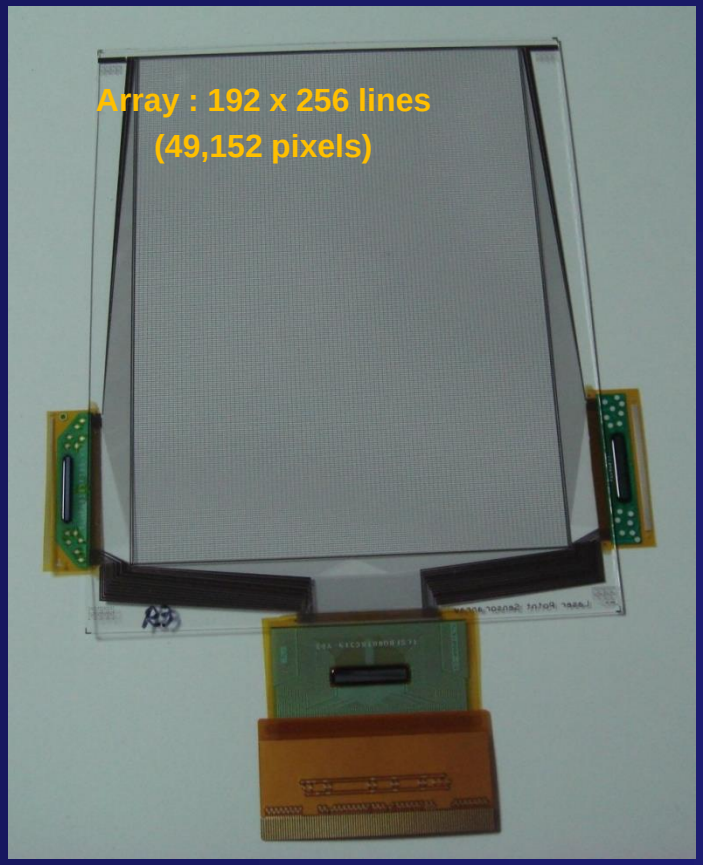
Fully Transparent Ox. Sensor Array





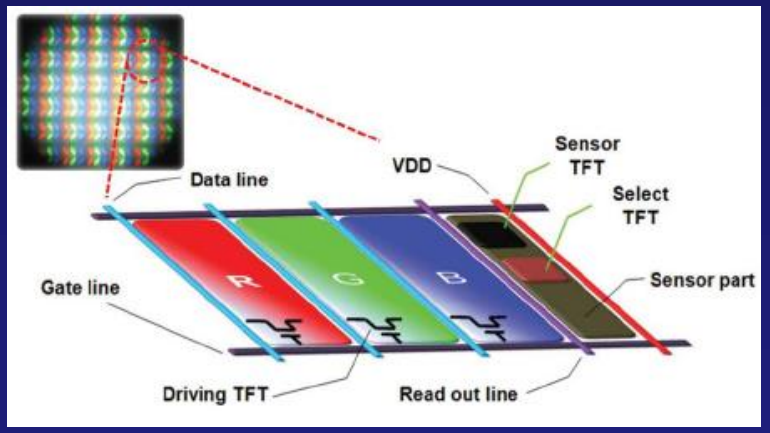
Demonstration of photo-sensor array and Interactive Display

Photo-sensor in 2010



S. Jeon, Nature Materials

Interactive Display in 2011



S. Jeon IEDM 2010, Adv. Mat. 2012, SID 2012

Summary

- NC-oxide semiconductor devices present various device applications.
- We proposes a novel hybrid CMOS image sensor utilizing oxide TFT and demonstrating excellent device performance of 180nm L_g TFT for future high density CIS devices.
- We present the three-dimensionally alternating integration of stackable logic devices with memory cells
- We present high performance bilayer oxide semiconductor such as HfInZnO/InZnO transistor for high power application
- We have integrated photo-TFTs in a transparent active-matrix photosensor array that can be operated at high frame rates and that has potential applications in contact-free interactive displays